Application No. 09/710,192
Amendment dated October 8, 2004
In Response to Notice of Non-Compliant Amendment dated September 29, 2004

**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1-13. (cancelled)

14. (currently amended) In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a first allocated channel information, including data addresses, corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a second allocated channel information, including data addresses, corresponding to said data transfer operation from said data streamer to a destination module; [and]

a buffer memory allocated to said data transfer operation for receiving data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information[.]; and

a buffer state memory configured to store a relationship which determines that said first channel information and said second channel information and said buffer memory is

used in said data transfer operation.

15. (previously presented)The data streamer in accordance with claim 14 wherein said channel state memory stores information corresponding to a plurality of data transfer operations between said modules.

16. (previously presented)The data streamer in accordance with claim 14, wherein a buffer memory is allocated for each one of said data transfer operations and the size of said buffer memory variably changes in accordance with the size of data in a corresponding data transfer operation.

17. (previously presented)The data streamer in accordance with claim 16 wherein the data transfer rate from a source module to a corresponding buffer in said buffer memory, is different than the data transfer rate from said buffer memory to a destination module.

18. (previously presented)The data streamer in accordance with claim 17 wherein said first allocated channel information includes a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor.

19. (previously presented)The data streamer in accordance with claim 18, wherein

said second allocated channel information includes a second channel descriptor, wherein said data transfer operation from said buffer to said destination module is accomplished in accordance with said second channel descriptor.

20. (currently amended) ~~The data streamer in accordance with claim 19, wherein~~ In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between said modules comprises:

a channel state memory configured to store a first allocated channel information, including a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor, said first channel information corresponding to a data transfer operation from a source module to said data streamer, and further configured to store a second allocated channel information, including a second channel descriptor, wherein said data transfer operation from said buffer to said destination module is accomplished in accordance with said second channel descriptor, said second channel information corresponding to said data transfer operation from said data streamer to a destination module, said first and said second channel descriptors having[e] a different format and wherein the data transfer rate from a source module to a corresponding buffer in said buffer memory, is different than the data transfer rate from said buffer memory to a destination module ; and

a buffer memory allocated to each one of said data transfer operation for receiving

data provided by said source module in accordance with said first allocated channel information and providing said received data to said destination module in accordance with said second allocated channel information, and wherein the size of said buffer memory variably changes in accordance with the size of data in a corresponding data transfer operation.

21. (previously presented)The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

22. (previously presented)The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent no-allocation policy.

23. (previously presented)The data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a non-coherent no-allocation policy.

24 -32 (cancelled without prejudice)

33. (previously presented)In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a

method for performing data transfer operations between said modules comprising the steps of:

storing a first allocated channel information, including data addresses,

corresponding to a data transfer operation from a source module to a buffer memory;

storing a second allocated channel information, including data addresses,

corresponding to said data transfer operation from said buffer memory to a destination module;

receiving data provided by said source module in accordance with said first allocated channel information; [and]

providing said received data to said destination module in accordance with said second allocated channel information[.]; and

storing a relationship in a buffer state memory which determines that said first channel information and said second channel information and said buffer memory is used in said data transfer operation.

34. (previously presented)The method in accordance with claim 33 further comprising the step of storing a plurality of said channel information each of which corresponding to a data transfer operation.

35. (previously presented)The method in accordance with claim 34, further comprising the step of allocating a buffer memory space within said buffer memory , and changing the size of said buffer memory space in accordance with the size of data in a corresponding data transfer operation.

36. (previously presented)The method in accordance with claim 35 further comprising the step of setting the data transfer rate from a source module to a corresponding buffer memory space at a different rate than the data transfer rate from said buffer memory space to a destination module.

37. (previously presented)The method in accordance with claim 36, further comprising the step of transferring data in accordance with a predetermined channel descriptor.

38. (previously presented)The method in accordance with claim 37 data streamer in accordance with claim 14 wherein said data transfer operation from a source module to a destination module includes a data cache operation having a coherent allocation policy.

39. (previously presented)The data streamer in accordance with claim 33 further comprising the step of providing data transfers having a data cache operation with a coherent no-allocation policy.

40. (previously presented)The data streamer in accordance with claim 33 further comprising the step of providing data transfers having a data cache operation with a non-coherent no-allocation policy.

41 - 67. (cancelled without prejudice).

68. (new) In an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a method for performing data transfer operations between said modules comprising the steps of:

storing a first allocated channel information, including a first channel descriptor, wherein said data transfer operation from a source module to said buffer is accomplished in accordance with said first channel descriptor, said first channel information corresponding to a data transfer operation from a source module to a buffer memory;

storing a second allocated channel information, including a second channel descriptor, wherein said data transfer operation from said buffer to said destination module is accomplished in accordance with said second channel descriptor, said second channel information corresponding to said data transfer operation from said buffer memory to a destination module, said first and said second channel descriptors having a different format;

receiving data provided by said source module in accordance with said first allocated channel information; and

providing said received data to said destination module in accordance with said second allocated channel information, wherein the data transfer rate from a source module to a corresponding buffer in said buffer memory, is different than the data transfer rate from said buffer memory to a destination module and wherein the size of said buffer memory variably changes in accordance with the size of data in a corresponding data transfer operation.